## REMARKS/ARGUMENTS

Claims 44, 48, 49 and 60-68 are currently pending, of which claims 44, 61, and 65 are the independent claims. Claims 1-43, 45-47, and 50-59 were previously cancelled. No new claims are added herein, and no claims are amended or newly cancelled herein. No new matter is believed to have been introduced to the application by this paper. Reconsideration and further examination are respectfully requested.

### *Claim Rejections – 35 USC § 103*

Claims 44, 61, and 65 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U. S. Pat. No. 6,278,193 ("Coico") in view of U. S. Pat. No. 5,528,825 ("Miyauchi") and Japanese Pat. Pub. No. JP362169448A ("Hiromasa"). Claims 48, 49, 60, 62-64, and 66-68 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Coico, Miyauchi and Hiromasa and further in view of the Flip Chip Ball Grid Array (FPBGA) Package Family reference ("Flip Chip"). Claims 44, 61, and 65 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Coico, Miyauchi [sic] and Hiromasa. In this regard, this rejection as stated at Item 3 on p.6 of the Office Action, references "Hikita et al. (US 5528825)", however, U.S. Pat. No. 5,528,825 is the "Miyauchi" patent, not "Hikita." Claims 48, 49, 60, 62-64, and 66-68 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Coico, Miyauchi and Hiromasa and further in view of Flip Chip. Reconsideration and withdrawal of these rejections are respectfully requested.

Independent Claim 44 is directed to a circuit component comprising a substrate and a semiconductor chip over a top surface of said substrate. The semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface. The semiconductor chip comprises multiple pads at said front surface. An identity of product is directly on said back surface of said semiconductor chip. Multiple metal bumps are between said multiple pads of said semiconductor chip and said top surface of said substrate. An optically transparent layer is vertically over said identity of product. The identity of product is visible through said optically transparent layer.

Independent Claim 61 is directed to a circuit component comprising a substrate and a semiconductor chip over a top surface of said substrate. The semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface.

The semiconductor chip comprises multiple pads at said front surface. An identity of manufacturer is directly on said back surface of said semiconductor chip. Multiple metal bumps are between said multiple pads of said semiconductor chip and said top surface of said substrate. An optically transparent layer is vertically over said identity of manufacturer, wherein said identity of manufacturer is visible through said optically transparent layer.

Independent Claim 65 is directed to a circuit component comprising a substrate and a semiconductor chip over a top surface of said substrate. The semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface. The semiconductor chip comprises multiple pads at said front surface. A bar code is directly on said back surface of said semiconductor chip. Multiple metal bumps are between said multiple pads of said semiconductor chip and said top surface of said substrate. An optically transparent layer is vertically over said bar code. The bar code is visible through said optically transparent layer.

The applied references, either alone or in combination, are not seen to teach or suggest the foregoing combination of features of each of independent Claims 44, 61, and 65.

The Office Action refers to Coico for teaching many features of Claim 44, but acknowledges that Coico fails to disclose or suggest "an identity of product directly on said back surface of said semiconductor chip and an optically transparent layer vertically over said identity of product," as recited in independent claim 44. Such rejection is apparently also applied by the Examiner to "said identity of manufacturer," as recited in independent claim 61, and "said bar code," as recited in independent claim 65. See Office Action, p. 3.

The Office Action then refers to Miyauchi [sic] as allegedly teaching that "barcodes can be printed directly onto each IC 10 or on the package (col 3 lines 6+)." See Office Action, p. 3. The Office Action also refers to Hiromasa for allegedly teaching an optically transparent layer vertically over said identity of product, and that it would have been obvious to combine the teachings of Coico, Miyauchi and Hiromasa to arrive at the combination of features of Claim 44.

Applicants respectfully disagree with this characterization of the references and submit that one of ordinary skill in the art would not have been motivated to combine the teachings of these references to arrive at the claimed invention.

First, Applicants submit that Miyauchi is only seen to disclose that a bar code is printed on the outside of the IC package. See Miyauchi, Fig. 3; col. 3, lines 9-12. Miyauchi is not seen to teach or disclose that an identity of product is provided directly on said back surface of said semiconductor chip, wherein multiple metal bumps are between the multiple pads of the semiconductor chip and the top surface of the substrate.

In addition, Hiromasa is not seen to teach or disclose "an optically transparent layer vertically over said identity of product." In this regard, the Office Action merely refers to the "abstract and constitution" of Hiromosa for allegedly teaching these features and does not provide any specific citation for each of these features allegedly shown in Hiromasa. In the "Constitution" section of the Abstract of Hiromasa, it is mentioned that "the thin film of transparent resin 4 is coated on the above-mentioned surface" in the recessed part 3 of package 2. See Hiromasa, "Constitution" section, and Fig. 1. However, Hiromasa is not seen to disclose a transparent layer through which can be observed a product identity/information directly on a back surface of a semiconductor chip. In this regard, Fig. 32 of the instant application shows that the marking (indicia IM) is directly on the back surface of a semiconductor chip (CH2) and that the marking (indicia IM) is also under the protection layer (PL2) that covers semiconductor chip (CH2). Thus, the marking of the instant application is located between the chip and the protective layer of the overall package; whereas, in contrast, the marking in Hiromasa is seen to be on top of the entire package 2 and then has a resin layer provided over the marking on the package. None of the references are seen to provide any motivation or suggestion to make such a combination of the claimed invention.

Accordingly, independent claims 44, 61, and 65 are believed to be allowable over the applied references. Reconsideration and withdrawal of the rejection of independent claims 44, 61, and 65 are respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the

arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

## CONCLUSION

In view of the remarks set forth herein, Applicant submits that the application is in condition for allowance and respectfully requests a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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